

# DATA SHEET

**74F30**

8-input NAND gate

Product specification

1989 Mar 03

IC15 Data Handbook

8-input NAND gate

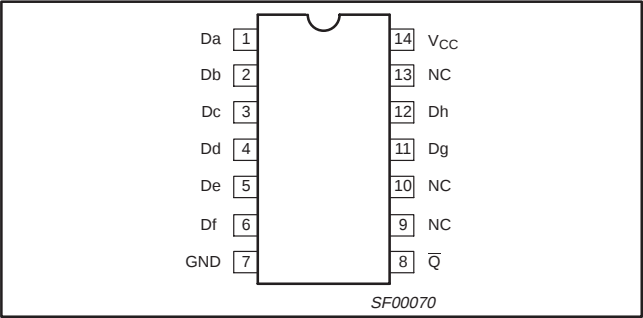
74F30

| TYPE  | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|-------|---------------------------|--------------------------------|
| 74F30 | 3.2ns                     | 1.7mA                          |

ORDERING INFORMATION

| DESCRIPTION        | COMMERCIAL RANGE<br>V <sub>CC</sub> = 5V ±10%,<br>T <sub>amb</sub> = 0°C to +70°C | PKG DWG # |
|--------------------|-----------------------------------------------------------------------------------|-----------|
| 14-pin plastic DIP | N74F30N                                                                           | SOT27-1   |
| 14-pin plastic SO  | N74F30D                                                                           | SOT108-1  |

PIN CONFIGURATION

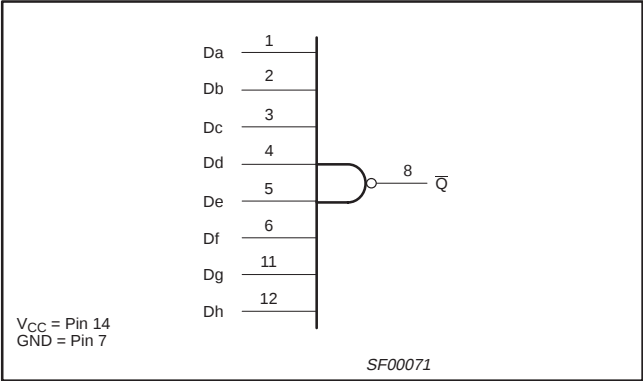


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

| PINS      | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-----------|-------------|---------------------|---------------------|
| Dn        | Data inputs | 1.0/1.0             | 20μA/0.6mA          |
| $\bar{Q}$ | Data output | 50/33               | 1.0mA/20mA          |

NOTE: One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

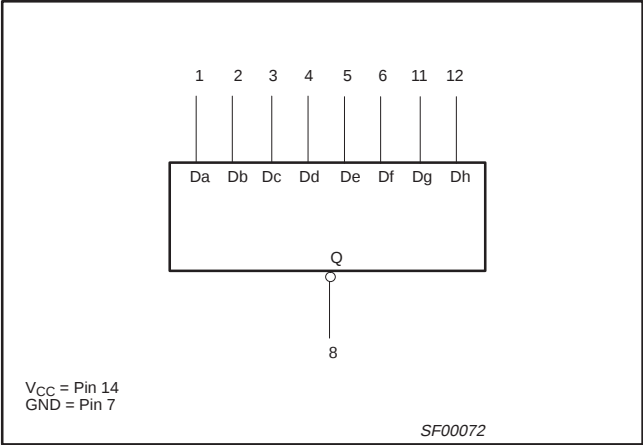


FUNCTION TABLE

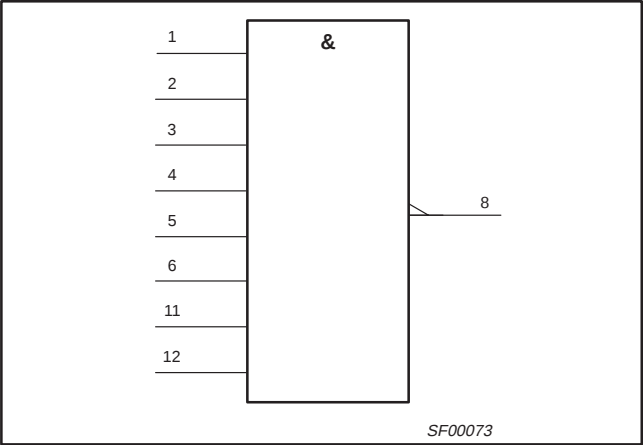
| INPUTS |     |     |     |     |     |     |     | OUTPUT     |
|--------|-----|-----|-----|-----|-----|-----|-----|------------|
| Dna    | Dnb | Dnc | Dnd | Dne | Dnf | Dng | Dnh | $\bar{Q}n$ |
| L      | X   | X   | X   | X   | X   | X   | X   | H          |
| X      | L   | X   | X   | X   | X   | X   | X   | H          |
| X      | X   | L   | X   | X   | X   | X   | X   | H          |
| X      | X   | X   | L   | X   | X   | X   | X   | H          |
| X      | X   | X   | X   | L   | X   | X   | X   | H          |
| X      | X   | X   | X   | X   | L   | X   | X   | H          |
| X      | X   | X   | X   | X   | X   | L   | X   | H          |
| H      | H   | H   | H   | H   | H   | H   | H   | L          |

- NOTES:
1. H = High voltage level
  2. L = Low voltage level
  3. X = Don't care

LOGIC SYMBOL



IEC/IEEE SYMBOL



## 8-input NAND gate

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL           | PARAMETER                                      | RATING                  | UNIT |
|------------------|------------------------------------------------|-------------------------|------|
| V <sub>CC</sub>  | Supply voltage                                 | −0.5 to +7.0            | V    |
| V <sub>IN</sub>  | Input voltage                                  | −0.5 to +7.0            | V    |
| I <sub>IN</sub>  | Input current                                  | −30 to +5               | mA   |
| V <sub>OUT</sub> | Voltage applied to output in High output state | −0.5 to V <sub>CC</sub> | V    |
| I <sub>OUT</sub> | Current applied to output in Low output state  | 40                      | mA   |
| T <sub>amb</sub> | Operating free-air temperature range           | 0 to +70                | °C   |
| T <sub>stg</sub> | Storage temperature range                      | −65 to +150             | °C   |

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL           | PARAMETER                            | LIMITS |     |     | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
|                  |                                      | MIN    | NOM | MAX |      |
| V <sub>CC</sub>  | Supply voltage                       | 4.5    | 5.0 | 5.5 | V    |
| V <sub>IH</sub>  | High-level input voltage             | 2.0    |     |     | V    |
| V <sub>IL</sub>  | Low-level input voltage              |        |     | 0.8 | V    |
| I <sub>IK</sub>  | Input clamp current                  |        |     | −18 | mA   |
| I <sub>OH</sub>  | High-level output current            |        |     | −1  | mA   |
| I <sub>OL</sub>  | Low-level output current             |        |     | 20  | mA   |
| T <sub>amb</sub> | Operating free-air temperature range | 0      |     | +70 | °C   |

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL          | PARAMETER                                 | TEST CONDITIONS <sup>1</sup>                                                                 |                                           | LIMITS                 |                  |              | UNIT |
|-----------------|-------------------------------------------|----------------------------------------------------------------------------------------------|-------------------------------------------|------------------------|------------------|--------------|------|
|                 |                                           |                                                                                              |                                           | MIN                    | TYP <sup>2</sup> | MAX          |      |
| V <sub>OH</sub> | High-level output voltage                 | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX<br>V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX | ±10%V <sub>CC</sub><br>±5%V <sub>CC</sub> | 2.5<br>2.7             |                  |              | V    |
| V <sub>OL</sub> | Low-level output voltage                  | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX<br>V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX | ±10%V <sub>CC</sub><br>±5%V <sub>CC</sub> |                        | 0.30<br>0.30     | 0.50<br>0.50 | V    |
| V <sub>IK</sub> | Input clamp voltage                       | V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>                                      |                                           |                        | -0.73            | -1.2         | V    |
| I <sub>I</sub>  | Input current at maximum input voltage    | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V                                                 |                                           |                        |                  | 100          | μA   |
| I <sub>IH</sub> | High-level input current                  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V                                                 |                                           |                        |                  | 20           | μA   |
| I <sub>IL</sub> | Low-level input current                   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V                                                 |                                           |                        |                  | -0.6         | mA   |
| I <sub>OS</sub> | Short-circuit output current <sup>3</sup> | V <sub>CC</sub> = MAX                                                                        |                                           | -60                    |                  | -150         | mA   |
| I <sub>CC</sub> | Supply current (total)                    | I <sub>CCH</sub>                                                                             | V <sub>CC</sub> = MAX                     | V <sub>IN</sub> = GND  |                  | 0.6          | mA   |
|                 |                                           | I <sub>CCL</sub>                                                                             |                                           | V <sub>IN</sub> = 4.5V |                  | 2.8          |      |

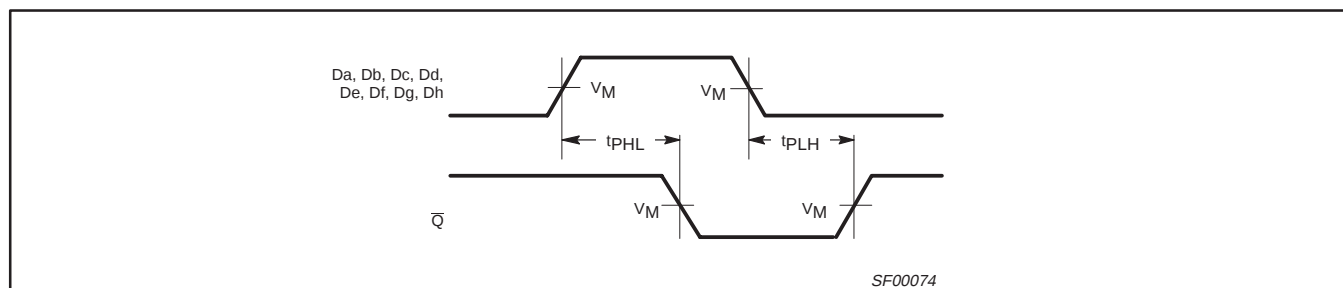
## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL                               | PARAMETER                                                             | TEST<br>CONDITION | LIMITS                                                                                              |            |            |                                                                                                                  |            |    | UNIT |
|--------------------------------------|-----------------------------------------------------------------------|-------------------|-----------------------------------------------------------------------------------------------------|------------|------------|------------------------------------------------------------------------------------------------------------------|------------|----|------|
|                                      |                                                                       |                   | V <sub>CC</sub> = +5.0V<br>T <sub>amb</sub> = +25°C<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |            | V <sub>CC</sub> = +5.0V ± 10%<br>T <sub>amb</sub> = 0°C to +70°C<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |    |      |
|                                      |                                                                       |                   | MIN                                                                                                 | TYP        | MAX        | MIN                                                                                                              | MAX        |    |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Da, Db, Dc, Dd, De, Df, Dg, Dh to $\overline{Q}$ | Waveform 1        | 1.5<br>1.0                                                                                          | 3.5<br>3.0 | 5.0<br>4.5 | 1.5<br>1.0                                                                                                       | 5.5<br>5.0 | ns |      |

## AC WAVEFORMS



Waveform 1. Propagation Delay for Inverting Outputs

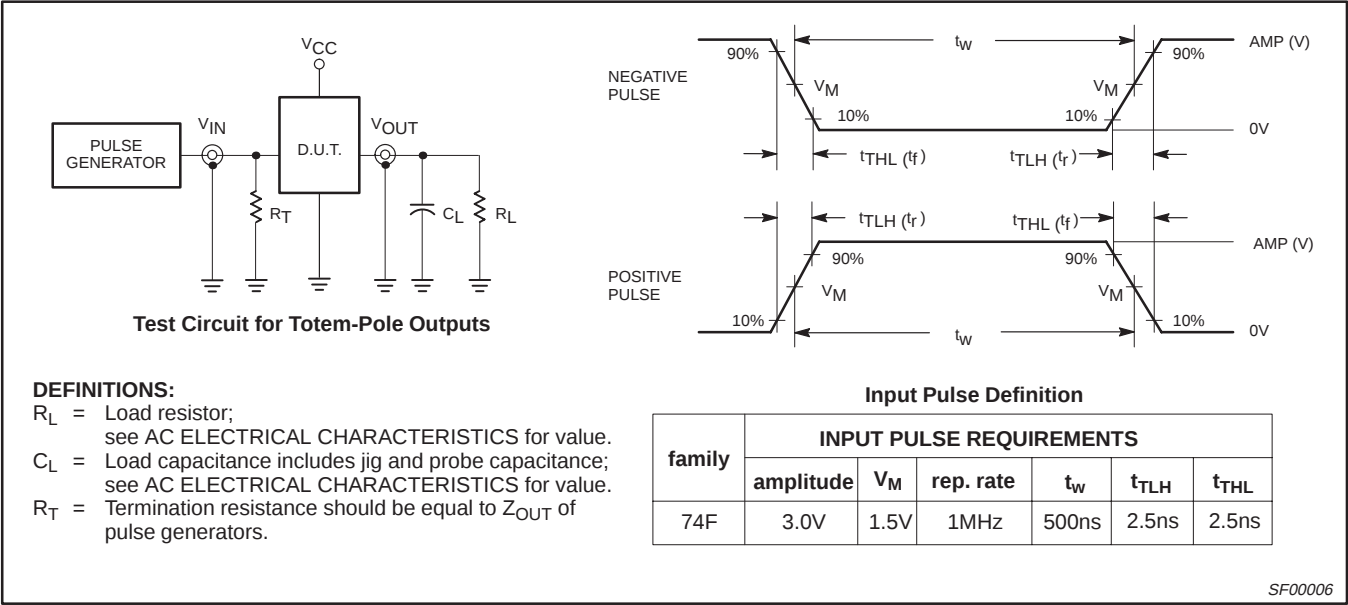
## NOTE:

For all waveforms, V<sub>M</sub> = 1.5V.

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TEST CIRCUIT AND WAVEFORMS

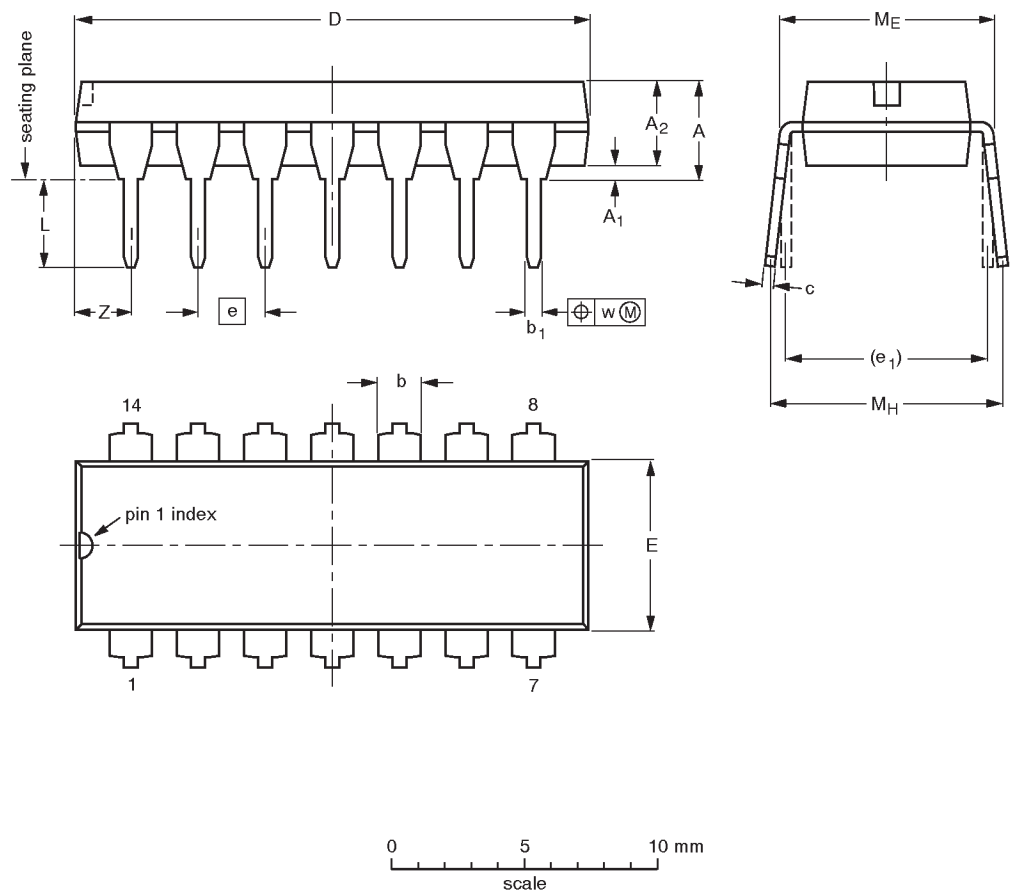


8-input NAND gate

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A<br>max. | A <sub>1</sub><br>min. | A <sub>2</sub><br>max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup><br>max. |
|--------|-----------|------------------------|------------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|--------------------------|
| mm     | 4.2       | 0.51                   | 3.2                    | 1.73<br>1.13   | 0.53<br>0.38   | 0.36<br>0.23   | 19.50<br>18.55   | 6.48<br>6.20     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.2                      |
| inches | 0.17      | 0.020                  | 0.13                   | 0.068<br>0.044 | 0.021<br>0.015 | 0.014<br>0.009 | 0.77<br>0.73     | 0.26<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.087                    |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

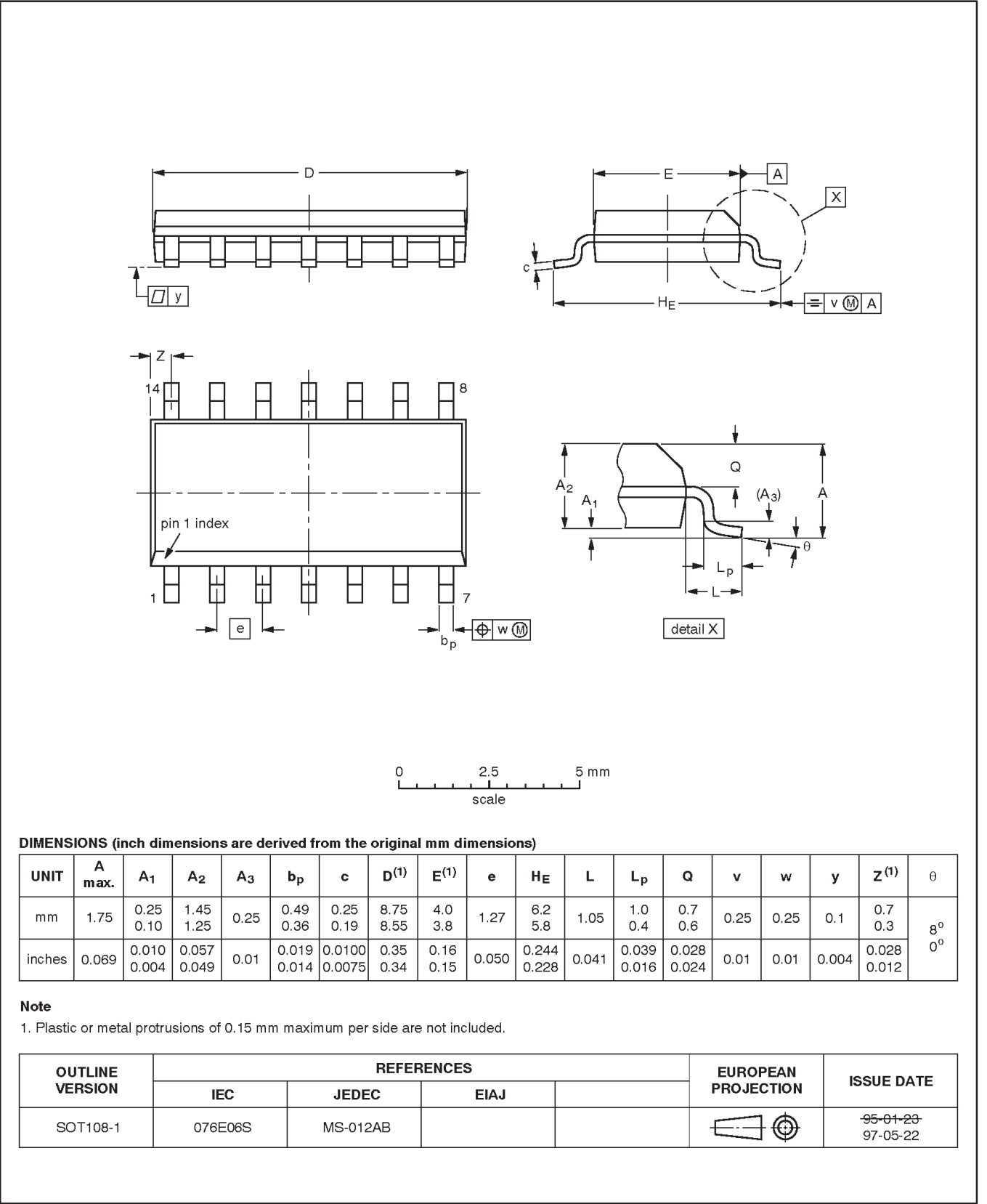
| OUTLINE<br>VERSION | REFERENCES |          |      |  | EUROPEAN<br>PROJECTION                                                                | ISSUE DATE           |
|--------------------|------------|----------|------|--|---------------------------------------------------------------------------------------|----------------------|
|                    | IEC        | JEDEC    | EIAJ |  |                                                                                       |                      |
| SOT27-1            | 050G04     | MO-001AA |      |  |  | 92-11-17<br>95-03-11 |

8-input NAND gate

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



## 8-input NAND gate

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## Data sheet status

| Data sheet status         | Product status | Definition [1]                                                                                                                                                                                                                                             |
|---------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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